IN THE CLAIMS:

Claim 12 has been added. Claims 2, 4, and 11 have been cancelled. Claims 1, 6, 7, 9 and 10 have been amended, as follows:

1. (currently amended) A data transfer control device for controlling data transfer between a first memory having a predetermined storage capacity ~~whose storage capacity is arbitrarily set~~ and a second memory corresponding to a buffer memory incorporated in a peripheral module, said data transfer control device comprising:

a first register for storing a first value representing a first number of times ~~for performing data transfer to suit a storage capacity of the second memory~~, by which data transfer is performed from the first memory to the second memory, the first value being determined based on a number of bits of data being output from the first memory and a storage capacity of the second memory;

a second register for storing a second value representing a second number of times ~~for performing data transfer to match an amount of transferring data stored in the first memory~~ by which data transfer is performed from the first memory to the second memory, the second value being determined based on an amount of data being stored in the first memory and being transferred to the second memory and the number of bits of data being output from the first memory; and

a controller for controlling ~~transferring of m-bit data (where 'm' is an integer arbitrarily set) based on the first value while controlling writing operations for the second memory, and for determining a timing to output an interrupt signal based on the second value with respect to a Central Processing Unit managing the first memory storing the~~

~~transferring data~~ the data transfer from the first memory to the second memory in accordance with the first value and for outputting an interrupt signal to a when a value accumulating the number of times data transfer is performed from the first memory to the second memory matches the second value.

Claim 2 (cancelled).

3. (currently amended) A data transfer control device according to claim 1, wherein a size of the second register is set in accordance with the predetermined storage capacity of the first memory.

Claim 4 (cancelled).

5. (original) A data transfer control device according to claim 1, wherein the transferring data are sequentially transferred from the first memory to the second memory in accordance with a Direct Memory Access transfer.

6. (currently amended) A data transfer control device according to claim 1, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data, and m-bit data is the number of bits of data being output from the first memory.

7. (currently amended) A data transfer control method for controlling data transfer between a first memory ~~whose storage capacity is arbitrarily set~~ having a predetermined storage capacity and a second memory corresponding to a buffer memory incorporated in a peripheral module, said data transfer control method comprising the steps of:

setting a first value representing a first number of times ~~for performing data transfer to suit a storage capacity of the second memory~~ by which data transfer is

performed from the first memory to the second memory, the first value being determined based on a number of bits of data being output from the first memory and a storage capacity of the second memory;

setting a second value representing a second number of times ~~for performing data transfer to match an amount of transferring data stored in the first memory~~ , by which data transfer is performed from the first memory to the second memory, the second value being determined based on an amount of data being stored in the first memory and being transferred to the second memory and the number of bits of data being output from the first memory;

controlling transferring of ~~m-bit data (where 'm' is an integer arbitrarily set) based on the first value while controlling writing operations for the second memory~~ the data from the first memory to the second memory in accordance with the first value; and

outputting an interrupt signal ~~based on the second value with respect to a Central Processing Unit managing the first memory storing transferring data~~ when a value accumulating a number of times data is transferred from the first memory to the second memory reaches the second value.

8. (original) A data transfer control method according to claim 7, wherein the transferring data are sequentially transferred from the first memory to the second memory in accordance with a Direct Memory Access transfer.

9. (currently amended) A data transfer control method according to claim 7, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data and m-bit data is

the number of bits of data being output from the first memory.

10. (currently amended) A data transfer control method according to claim 7, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data, so that the n-byte data are collectively transferred from the first memory to the second memory by sequentially transferring the m-bit data the first number of times so as to satisfy the storage capacity of the second memory and m-bit data is the number of bits of data being output from the first memory.

Claim 11 (cancelled).

12. (new) A data transfer control device according to claim 1, wherein the first value is produced by dividing the storage capacity of the second memory by the number of bits of data being output from the first memory, and the second value is produced by dividing the amount of data being stored in the first memory and being transferred to the second memory by the number of bits of data being output from the first memory.